IN THE CLAIMS:

Please cancel Claims 1-28 without prejudice.

Please add the following newly drafted Claims 29-39.

1.- 28. (Cancelled)

29. (New) A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor has only the first conditional instruction out of the first and second conditional instructions.

30. (New) The processor of Claim 29,

wherein the first conditional instruction is a conditional transfer instruction.

31. (New) The processor of Claim 29,

wherein the first conditional instruction is a conditional arithmetic instruction.

32. (New) A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor is operable to decode only the first conditional instruction out of the first and second conditional instructions.

33. (New) The processor of Claim 32,

wherein the first conditional instruction is a conditional transfer instruction

34. (New) The processor of Claim 32

wherein the first conditional instruction is a conditional arithmetic instruction

35. (New) A processor for executing an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second conditional instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions,

wherein the processor is operable to execute only the first conditional instruction out of the first and second conditional instructions.

36. (New) The processor of Claim 35,

wherein the first conditional instruction is a conditional transfer instruction

37. (New) The processor of Claim 35 wherein the first conditional instruction is a conditional arithmetic instruction

38. (New) A processor that executes an instruction sequence, comprising:

a decoding unit operable to decode an instruction sequence generated by converting a program that is capable of being described by mutually exclusive first and second

conditionally instructions, so that the instruction sequence includes only the first conditional instruction out of the first and second conditional instructions;

an executing unit operable to execute the instruction sequence decoded by the decoding unit;

wherein the decoding unit is operable to decode only the first conditional instruction out of the first and second conditional instructions.

39. (New) An instruction conversion apparatus for converting a program that is capable of being described by mutually exclusive first and second conditional instructions into an instruction sequence executable by a processor,

wherein the instruction conversion apparatus, when only the first conditional instruction out of the first and second conditional instructions is decodable by the processor, interchanges (a) a condition of the second conditional instruction with a condition of the first conditional instruction, and (b) an instruction executed when the condition of the second conditional instruction is satisfied with an instruction executed when the condition of the second conditional instruction is satisfied with an instruction executed when the condition of the second conditional instruction is not satisfied.

40. (New) An instruction conversion apparatus comprising:

an intermediate code generating unit operable to generate an intermediate code sequence by converting a program that is capable of being described by mutually exclusive first and second conditional instructions;

a detecting unit operable to detect, from the intermediate code sequence, (a) a conditional instruction that judges whether to execute one of a first operation and a second operation, (b) a first operation code that executes an instruction when the judgment result of the conditional instruction is to execute the first operation, and (c) a second operation code that executes an instruction when the judgment result of the conditional instruction is to execute the second operation; and

an interchanging unit operable, when only the first conditional instruction out of the first and second conditional instruction is decodable by a processor, to interchange (a) the second conditional instruction with the first conditional instruction, and (b) an operation of the first operation with an operation of the second operation.